

Temperature performance of AlGaIn/GaN MOS-HEMTs

on Si substrates using Gd₂O₃ as gate dielectric

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GaN based high electron mobility transistors have draw great attention due to its potential in high temperature, high power and high frequency applications [1, 2]. However, significant gate leakage current is still one of the issues which need to be solved to improve the performance and reliability of the devices [3]. Several research groups have contributed to solve this problem by using metal–oxide–semiconductor HEMTs (MOSHEMTs), with a thin dielectric layer, such as SiO₂ [4], Al₂O₃ [5], HfO₂ [6] and Gd₂O₃ [7] between the gate and the barrier layer on AlGaIn/GaN heterostructures. Gd₂O₃ has shown low interfacial density of states(D_{it}) with GaN and a high dielectric constant and low electrical leakage currents [8], thus is considered as a promising candidate for the gate dielectrics on GaN. MOS-HEMTs using Gd₂O₃ grown by electron-beam heating [7] or molecular beam epitaxy (MBE) [8] on GaN or AlGaIn/GaN structure have been investigated, but further research is still needed in Gd₂O₃ based AlGaIn/GaN MOSHEMTs.

The high-temperature operation of AlGaIn/GaN HEMTs on Si has been evaluated previously by several groups [9, 10]. However, there has been very little work on the thermal stability of insulated-gate AlGaIn/GaN structures on Si substrates for high-temperature applications.

In this work, thermal stability of Gd₂O₃ based AlGaIn/GaN MOSHEMTs on Si substrates were studied and compared with standard AlGaIn/GaN HEMTs.

A thin layer of Gd₂O₃ with (4.2 ± 0.3 nm) thickness and 2.1 nm root mean square (RMS), was deposited using high pressure sputtering technique [11] as the gate dielectric of AlGaIn/GaN based HEMTs. IV DC and pulse characterization was carried out at room temperature (RT). The MOSHEMTs transistors showed an OFF-state (V_{GS}=-8 V) drain-source leakage current density at V_{DS} =15 V of 1.1×10⁻⁴ A/cm², which is about four orders of magnitude lower than in the conventional, reference HEMTs. However, no significant differences were observed in the saturation drain-source current density (I_{DSS}) (0.63±0.3 A/mm) and peak transconductance (g_{m,max}) (135±5 mS/mm) for both kinds of devices. In addition, both the

MOSHEMTs and HEMTs showed similar gate lag ratios, which could be attributed to trapped charges in the unpassivated area between gate and drain.

The same electrical measurement procedure was conducted on the devices during and after a thermal cycle from RT to 425°C with a 100°C step. The results showed that the off-state drain source leakage current was quite stable (5 nA/mm) with increasing temperature in the MOSHEMTs, but it increased with a rate of one magnitude per 100°C (from 80 nA/mm at RT to 0.2 mA/mm at 425°C) in conventional HEMTs as shown in Fig. 1. Therefore, MOSHEMTs show better thermal stability than conventional HEMTs.

As expected, I_{DSS} and g_m decreased with increasing temperature for both MOSHEMTs and HEMTs, although the decrease in MOSHEMTs is 15% smaller than that of HEMTs. The threshold voltage showed a positive shift at high temperature in MOSHEMTs, and stays stable after the thermal cycle at RT (-4.4 V), which suggested that the thermal treatment contributed to improve the interface between the Gd_2O_3 layer and the AlGaIn/GaN heterostructure, while maintaining the low leakage current.

In conclusion, GaN-based MOSHEMTs with Gd_2O_3 are more suitable devices for high temperature applications than the conventional HEMTs, due to smaller and more stable gate leakage current up to ~400°C, and the lower decrease in I_{DSS} and $g_{m,max}$ during the device heating.

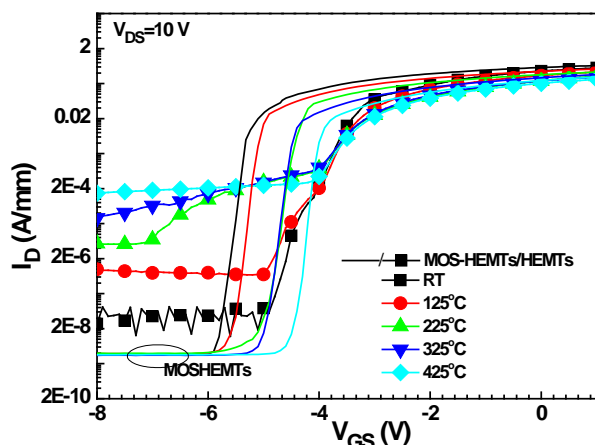


Figure 1: I_D - V_{GS} - T of the MOSHEMT (solid lines) and HEMT (symbol-lines) devices at $V_{DS} = 10$ V.

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References:

- [1] U. K. Mishra et al., Proceedings of the IEEE **96**, 287-305(2008)
- [2] J. Das et al., IEEE Electron Device Letters **32**, 1370-1372 (2011)
- [3] S. Mizuno et al., Japanese Journal of Applied Physics **41**, 5125(2002)
- [4] F. Husna et al., IEEE Transactions on Electron Devices **59**, 2424-2429(2012)
- [5] Z. H. Liu et al., Applied Physics Letters **98**, 163501(2011)
- [6] X. Sun et al., Applied Physics Letters **102**, 103504(2013)
- [7] A. Laha et al., Applied Physics Letters **90**, 113508(2007)
- [8] W. Chang et al., Journal of Crystal Growth **311**, 2183-2186(2009)
- [9] C.H. Chen et al., Microelectronics Reliability **52**, 2551-2555(2012)
- [10] E. Zanoni et al., ECS Transactions **41**, 237-249(2011)
- [11] E. San Andres et al., 2013 Spanish Conference on Electron Devices (CDE 2013), 25-2(2013)